REMARKS

The Applicant has carefully considered this application in connection with the Examiner's Action and respectfully requests reconsideration of this application in view of the foregoing amendments and the following remarks.

The Applicant originally submitted Claims 1-20 in the application. The Applicant affirms that Claims 6-10 were withdrawn from consideration as being non-elected claims, and are hereby cancelled pending the possible filing of a divisional application. Additionally, Claims 1, 4, 11 and 14 have been amended to further delineate an inherent feature of the previously claimed subject matter. Accordingly, Claims 1-5 and 11-20 are currently pending in the application.

I. Rejection of Claims under 35 U.S.C. §103

The Examiner has rejected Claims 1-4, 11-14 and 16-20 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,908,313 to Chau, *et al.* ("Chau") in view of U.S. Patent No. 6,724,660 to Stotnicki, *et al* ("Stotnicki"). With the exception of epitaxially growing a semiconductor material within a recess to form a source/drain region, the Examiner asserts that Chau teaches all of the other elements of independent Claims 1 and 11. The Examiner introduces Stotnicki for a teaching directed to epitaxially growing a semiconductor material within a recess to form a source/drain region. The Examiner asserts that it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the method shown in Chau with the teachings of Stotnicki directed to epitaxially growing the semiconductor

material to arrive at the claimed invention. In addressing the motivation to combine, the Examiner suggests that both Chau and Stotnicki are directed to reducing junction capacitance without surrendering read sensitivity. (Examiner's Action, page 4). For the reasons as stated below, the Applicant respectfully disagrees.

Chau is directed to a metal oxide semiconductor transistor with minimal junction capacitance. (Column 1, lines 5-6). A gate dielectric layer of the transistor is formed on a first surface of the semiconductor substrate with a gate electrode formed thereon. A pair of recesses are then formed in the semiconductor substrate on opposite sides of the gate electrode and a dielectric layer is thereafter formed on a surface of each of the recesses. A semiconductor material is deposited into the recesses to form a pair of source/drain regions. (Column 2, lines 37-46).

The dielectric layer essentially adds a capacitance in series with the junction capacitance of the transistor which in turn reduces the effective junction capacitance thereof. It is to be noted that the dielectric layer is formed within the recesses that ultimately form the source/drain regions, and is not formed beneath the channel regions or isolation regions underlying the gate dielectric layer. Additionally, the dielectric layer acts as barrier layer to prevent vertical dopant diffusion which allows abrupt source/drain junctions to be formed. (Column 4, lines 35-45).

The dielectric layer is formed by implanting nitrogen atoms into the recesses to form nitrogen doped silicon substrate regions in alignment with the outside edges of sidewall spacers about the gate electrode. A low energy nitrogen implant is used to place nitrogen atoms directly beneath a bottom surface of the recesses. The silicon substrate is only "doped" with nitrogen atoms in that the nitrogen atoms are not yet chemically reacted with the silicon of the silicon substrate to form the dielectric layer. (Column 6, lines 42-54).

To the contrary, the methods of forming a source/drain region in accordance with the inventions as recited in Claims 1 and 11 of the present application include forming a recess in a substrate adjacent a gate of a transistor and forming a conductive deep doped region below a bottom surface of the recess. The deep doped region, therefore, is a conductive region as opposed to the region formed within the recesses of the source/drain of Chau, which is a dielectric layer. Thus, in addition to not disclosing epitaxially growing a semiconductor material within a recess to form a source/drain region as admitted by the Examiner, Chau does not disclose, among other things, forming a conductive deep doped region below a bottom surface of the recess that accommodates the source/drain region.

Stotnicki fails to cure the deficiencies of Chau. Stotnicki is directed to an integrated semiconductor memory device including at least one integrated memory point structure including a quantum well semiconductor area buried in the substrate of the structure and disposed under an insulated gate of a transistor. (Column 1, lines 60-64). A method of constructing the memory point structure is illustrated and described with respect to FIGUREs 4a to 4g of Stotnicki. In accordance with the Examiner's assertion, Stotnicki does disclose selectively epitaxially growing silicon within a pair of lateral recesses located about the gate of the memory point structure. (Column 5, line 66 to column 6, line 27).

Analogous to Chau, however, Stotnicki also fails to disclose, among other things, forming a conductive deep doped region below a bottom surface of the recess that accommodates the source/drain region. Thus, Chau and Stotnicki, individually or in combination, fail to disclose, or even suggest, an element as recited in independent Claims 1 and 11 of the present application.

In view of the foregoing remarks, therefore, the cited references do not support the Examiner's rejection of Claims 1 and 11, and the claims dependent thereon, under 35 U.S.C. §103(a). In accordance therewith, the Applicant respectfully requests the Examiner withdraw the rejection.

II. Conclusion

In view of the foregoing amendments and remarks, the Applicant now sees all of the claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-5 and 11-20.

The Applicant requests that the Examiner to telephone the undersigned attorney of record at (972) 732-1001 if such would further expedite the prosecution of the present application.

Respectfully submitted,
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